CLAIMS

What is claimed is:

1. A method comprising:

forming a first via; and

stacking a second via onto the first via, at least one of the first via and the second via being a skip via.

2. The method of claim 1 wherein stacking a second via onto the first via includes stacking a second skip via onto a first skip via.

3. The method of claim 1 wherein stacking the second via onto the first via includes substantially aligning a longitudinal axis of the first via with a longitudinal axis of the second via.

4. The method of claim 1 wherein forming a first via comprises:

forming a first conductive layer onto a core;

forming a first dielectric layer such that the first conductive layer is between the first dielectric layer and the core;

forming a second conductive layer onto the first dielectric layer;

forming a second dielectric layer such that the second conductive layer is between the first dielectric layer and the second dielectric layer;

forming an opening in the first and second dielectric layers; and

forming a first skip via in the opening.

5. The method of claim 4 wherein forming an opening in the first and second dielectric layers includes drilling an opening in the first and second dielectric layers.

6. The method of claim 5 wherein drilling an opening in the first and second dielectric layers includes laser drilling an opening in the first and second dielectric layers.

7. The method of claim 4 wherein forming an opening in the first and second dielectric layers includes etching an opening in the first and second dielectric layers.

8. The method of claim 4 wherein forming a first conductive layer includes plating the first conductive layer onto the core and patterning the first conductive layer, and wherein forming a second conductive layer includes plating the second conductive layer onto the first dielectric layer and patterning the second conductive layer.

9. The method of claim 4 wherein forming the first skip via in the opening includes filling the opening with a conductive material.

10. The method of claim 9 wherein filling the opening with a conductive material includes forming a third conductive layer onto the second dielectric layer.

11. The method of claim 4 wherein forming a third conductive layer on the second dielectric layer includes patterning the third conductive layer.

12. The method of claim 10 further comprising:
forming a third dielectric layer on the third conductive layer;
forming a second opening in the third dielectric layer; and
forming the second via in the second opening.

13. The method of claim 12 wherein forming the second via in the second opening includes forming a fourth conductive layer onto the third dielectric layer.

14. A substrate comprising:
a plurality of dielectric layers;
a first skip via extending through two of the dielectric layers; and
a second via extending through one of the dielectric layers, the second via and the first skip via being stacked on top of one another.

15. The substrate of claim 14 wherein the second via is a second skip via extending through two of the dielectric layers.

16. The substrate of claim 14 wherein the first skip via includes a longitudinal axis and the second via includes a longitudinal axis, the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second via.

17. The substrate of claim 14 further comprising a third via extending through at least one of the dielectric layers, the third via being stacked onto the first skip via and the second via.

18. The substrate of claim 14 wherein the plurality of dielectric layers is formed on a core.

19. A computer system comprising:

a bus;

a memory coupled to the bus; and

a substrate electrically coupled to the bus, the substrate including a plurality of dielectric layers, a first skip via extending through two of the dielectric layers and a second via extending through one of the dielectric layers, the second via and the first skip via being stacked on top of one another.

20. The computer system of claim 19 wherein the second via is a second skip via extending through two of the dielectric layers.

21. The computer system of claim 19 further comprising a processor coupled to the substrate and the bus.